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Complete if Known **Application Number** 10/664,190 Filing Date September 16, 2003 First Named Inventor: Yervant Zorian et al. Art Unit 2138 **Examiner Name** Kerveros, James C. Attornou Docket Number

004640 0010

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Substitute for Form 1449/PTO Complete if Known 10/664,190 **Application Number** INFORMATION DISCLOSURE Filing Date September 16, 2003 STATEMENT BY APPLICANT First Named Inventor: Yervant Zorian et al. (use as many sheets as necessary) Art Unit 2138 **Examiner Name** Kerveros, James C. 004640.P019 **Sheet** of Attorney Docket Number NON PATENT LITERATURE DOCUMENTS T² Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Examiner Cite Initials* No1 item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published CHANG, Tsin-Yuan and ZORIAN, Yervant: "Tutorial 2: SoC Testing and P1500 Standard," Asian Test Symposium 2000: 492 JK MARINISSEN, Erik Jan, et. al.: "Wrapper Design for Embedded Core Test," ITC 2000: 911-920. ZORIAN, Yervant and SHOUKOURIAN, Samuel: "Embedded-Memory Test and Repair: Infrastructure IP for SoC Yield," IEEE CS and IEEE CASS May-June 2003: 58-66 BENSO, Alfredo, et. al.: "HD2BIST: a Hierarchical Framework for BIST Scheduling, Data Patterns Delivering and Diagnosis in SoCs," ITC 2000: 892-901 GIZOPOULOS, Dimitris, et. al.: "Low Power/Energy BIST Scheme for Datapaths," VTS 2000: 23-28 VARDANIAN, Valery A. and ZORIAN, Yervant: "A March-based Fault Location Algorithm for Static Random Access Memories," MDTD 2002: 256-261 BENSO, Alfredo, et. al., "HD-BIST: A Hierarchical Framework for BIST Scheduling and Diagnosis in SoCs," ITC 1999: 1038-1044

				 	
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